Spur Reduction Techniques for Phase-Locked Loops Exploiting A Sub-Sampling Phase Detector

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***Abstract*—This paper presents phase-locked loop (PLL) reference-spur reduction design techniques exploiting a sub-sampling phase detector (SSPD) (which is also referred to as a sampling phase detector). The VCO is sampled by the reference clock without using a frequency divider and an amplitude controlled charge pump is used which is inherently insensitive to mismatch. The main remaining source of the VCO reference spur is the periodic disturbance of the VCO by the sampling at the reference frequency. The underlying VCO sampling spur mechanisms are analyzed and their effect is minimized by using dummy samplers and isolation buffers. A duty-cycle-controlled reference buffer and delay-locked loop (DLL) tuning are proposed to further reduce the worst case spur level. To demonstrate the effectiveness of the proposed spur reduction techniques, a 2.21 GHz PLL is designed and fabricated in 0.18 μm CMOS technology. While using a high loop-bandwidth-to-reference-frequency ratio of 1/20, the reference spur measured from 20 chips is <-80 dBc. The PLL consumes 3.8 mW while the in-band phase noise is -121 dBc/Hz at 200 kHz and the output jitter integrated from 10 kHz to 100 MHz is 0.3 ps_{rms}.**

***Index Terms*—Clock generation, clock multiplier, clocks, frequency multiplication, frequency synthesizer, low jitter, low phase noise, low power, low spur, phase detector, phase-locked loop (PLL), sampling phase detector, sub-sampling phase detector.**

I. Introduction

A CLOCK with high spectral purity is required in many applications, e.g., in wireless communication systems to up-convert and down-convert the wanted signals and in analog-to-digital converters (ADCs) to accurately define the sampling moments. The spectral purity of the clock source is critical for the overall system performance. In addition to low phase noise, the clock source is often also required to have low spurious tones since clock spurs cause reciprocal mixing of the neighbor channels to the passband of the IF filter [1] or translate to deterministic jitter and degrade the ADC signal-to-noise ratio.

Phase-locked loops (PLLs) are widely used to generate high-accuracy clocks on chip. In conventional charge pump (CP) PLLs, the mismatch between the CP up-current source and down-current source is the major source for the reference spur at the voltage-controlled oscillator (VCO) output [2]–[8]. Mismatches in the CP current sources generate CP output-current ripple which is then converted to ripple on the VCO control voltage by the loop filter (LF), resulting in VCO spurs. A small filter bandwidth can be used to suppress the ripple, thereby reducing the VCO spur level. However, most PLL applications prefer a large bandwidth as it offers fast settling time, reduces on-chip filter area and reduces the sensitivity of the VCO to pulling [6]. In order to alleviate the tradeoff between low spur and large bandwidth, various design techniques have been proposed to reduce the CP ripple. Examples are CP designs that improve current source matching [2], [8], detect the current source mismatch and then apply analog [4] or digital [5] calibration, or designs that add a sample-and-hold between the CP and the loop filter [6], [7]. In this paper, we propose to use a sub-sampling PLL (SSPLL) architecture [9] and an amplitude controlled mismatch insensitive CP, which achieves a low reference spur <-80 dBc while using a high bandwidth of $f_{\text{ref}}/20$. The design with some measurements has been presented in [10]. Here we analyze the underlying spur mechanisms, discuss and analyze circuit operation in more detail and demonstrate more experimental proof of the concept.

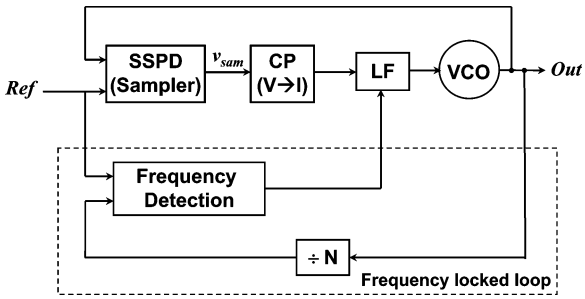

Fig. 1. Generic sub-sampling PLL (SSPLL) architecture.

The generic architecture of a SSPLL is shown in Fig. 1. A sub-sampling phase detector (SSPD) samples the VCO output with a reference clock Ref and converts the VCO phase error into sampled voltage variations. A CP converts sampled voltage to current and injects it to the loop filter. An auxiliary frequency-locked loop (FLL) guarantees correct frequency locking. The sub-sampling PD is not a recent invention, but has been used for a long time in various designs [11]–[16] under the name "sampling PD". The contribution of our work, as previously described in [9], is the development of techniques which allow a fully integrated CMOS PLL that exploits the sampling PD to achieve very low in-band phase noise. In [9] we demonstrated

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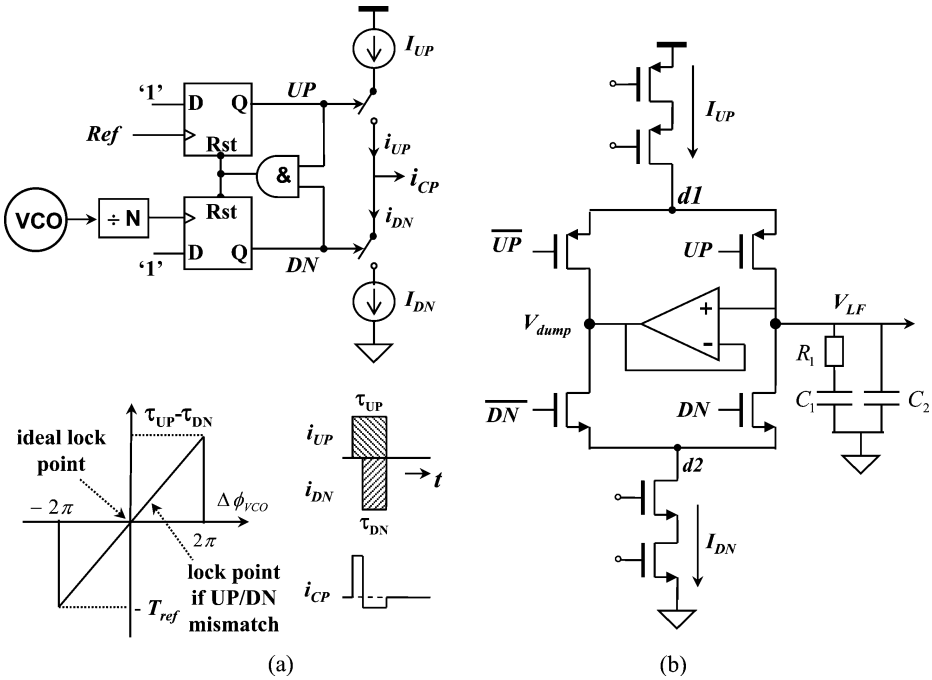

Fig. 2. (a) Three-state PFD and timing controlled CP. (b) Conventional low-ripple CP implementation.

that this integrated version of a sampling-based PLL has a great noise advantage over a classical PLL, especially when the frequency division ratio N is large, i.e., when a high-frequency VCO is sub-sampled by a low-frequency Ref. In order to emphasize this fact, we prefer to use the name "sub-sampling" in our work. Note that the noise benefit comes from the high detection gain of a SSPD/CP, due to the high slew-rate of the VCO. On the other hand, a very high SSPD/CP gain makes full integration difficult (i.e., limited loop filter capacitance). Therefore, [9] used a pulsed CP to lower the gain. Unlike a conventional CP, the on-time of this pulsed CP does *not* depend on the phase-difference, but is constant. The phase information is in the sampled voltage and the function of the CP is (time-windowed) voltage to current conversion. We will show in Section II-B of this paper that this CP is inherently insensitive to mismatch, due to its amplitude controlled nature. The CP design can thus be largely simplified while still producing small ripple. Although the SSPD and the amplitude controlled CP have already been used in [9], they did not lead to a low spur level there. We will show that this is because the SSPD periodically disturbs the VCO operation during sampling, causing actually large VCO spurs. The VCO sampling spur mechanisms will be analyzed in Section III and design techniques will be proposed to mitigate them. Different from the CP, the SSPD disturbs the VCO without going through the LF and hence there is no tradeoff between low SSPD spur and large PLL bandwidth. As a result, very low reference spur can be achieved while using a high PLL bandwidth. In addition to low reference spur, the proposed design also achieves low in-band phase noise and jitter with low power because the divider noise is eliminated and the SSPD and CP noise is not multiplied by N^2 in a SSPLL [9]. Circuit implementation consideration will be presented in Section IV. Section V presents the experimental results andSection VI gives conclusions.

II. Spur Due to Charge Pump

We will now first discuss the conventional CP and then the amplitude-controlled CP for the SSPLL, to explain why the latter is beneficial in terms of output current ripple generation.

A. Conventional CP

In PLL designs, the phase frequency detector (PFD) and CP as shown in Fig. 2(a) is often used. During operation, the PFD compares the phase of the divided-down VCO to the phase of Ref and generates two signals UP and DN to control the CP. It converts the VCO phase error into the on-time difference $\tau_{\rm UP}-\tau_{\rm DN}$ between the CP up-current source $I_{\rm UP}$ and down-current source $I_{\rm DN}$. In this conventional CP, $I_{\rm UP}$ and $I_{\rm DN}$ have a *variable on-time* but a *constant amplitude* fixed by biasing. When the PLL is phase locked, the net charge provided by the CP should be zero. To maintain the steady-state locking condition, the following equation must be satisfied:

$$I_{\rm UP}\cdot\tau_{\rm UP}=I_{\rm DN}\cdot\tau_{\rm DN}. \tag{1}$$

In case there is mismatch between the amplitudes of $I_{\rm UP}$ and $I_{\rm DN}$, we have $I_{\rm UP}\neq I_{\rm DN}$ and $\tau_{\rm UP}\neq\tau_{\rm DN}$. One of the CP current sources thus has to be on for a longer time in order to satisfy (1). This causes CP output current ripple as shown in Fig. 2(a), which is then converted to ripple on the VCO control voltage by the LF. If $i_{\rm CP,fref}$ is the amplitude of the fundamental component of the CP output current ripple, the corresponding VCO reference spur ${\rm SP}_{\rm fref,CP}$ can be calculated as [1]

$${\rm SP}_{\rm fref,CP}=20\log\frac{i_{\rm CP,fref}\cdot|F_{\rm LF}(j2\pi\cdot f_{\rm ref})|\cdot\dfrac{K_{\rm VCO}}{2\pi}}{2f_{\rm ref}} \tag{2}$$

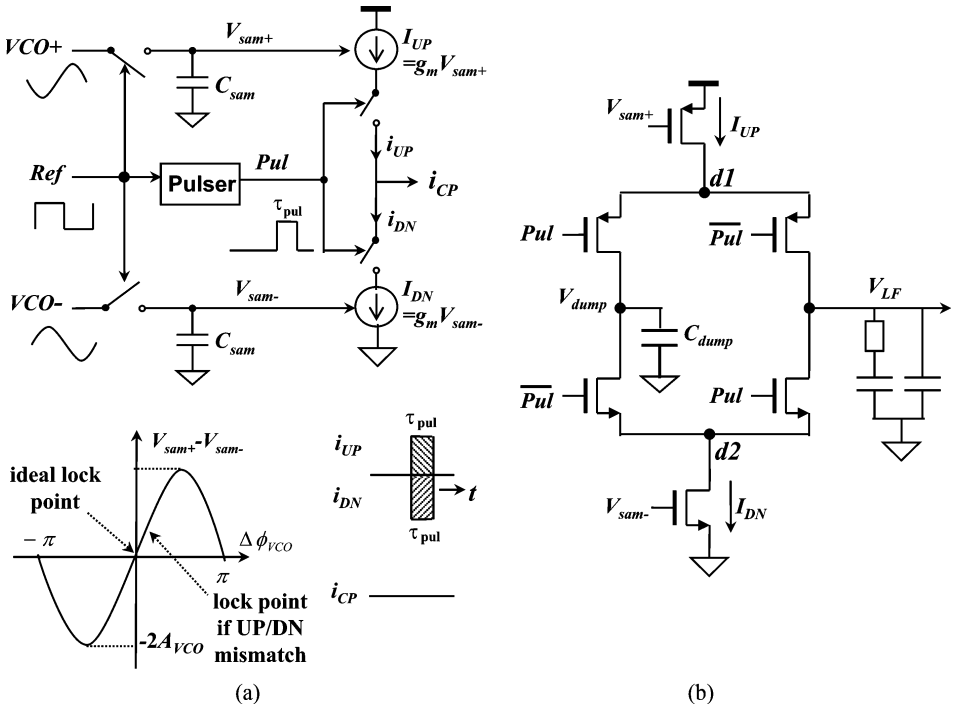

Fig. 3. (a) SSPD and amplitude-controlled CP. (b) Proposed low-ripple CP implementation.

where $F_{\rm LF}(s)$ is the LF transimpedance transfer function and $K_{\rm VCO}$ is the VCO analog tuning gain in rad/V. When the often-used second-order *RC* filter as in Fig. 2(b) is used, we have

$$F_{\rm LF}(s) = \frac{1}{(C_1+C_2)s}\cdot\frac{1+R_1C_1s}{1+R_1\cdot\dfrac{C_1C_2}{C_1+C_2}\cdot s} = \frac{1}{(C_1+C_2)s}\cdot\frac{1+\dfrac{s}{2\pi f_{\rm zero}}}{1+\dfrac{s}{2\pi f_{\rm pole}}} \quad (3)$$

where $f_{\rm zero}=1/2\pi R_1C_1$ and $f_{\rm pole}=1/(2\pi R_1C_1C_2/(C_1+C_2))$ are the LF zero and pole frequencies.

In most designs, we have $f_{\rm zero}<f_{\rm pole}\ll f_{\rm ref}$ and $C_1\gg C_2$. The VCO spur can then be approximated using (2) and (3) as

$$\mathrm{SP}_{\rm fref,CP}\approx 20\log\frac{i_{\rm CP,fref}\cdot R_1\cdot K_{\rm VCO}}{4\pi f_{\rm ref}}+20\log\frac{f_{\rm pole}}{f_{\rm ref}}. \quad (4)$$

Defining a CP feedback gain $\beta_{\rm CP}$ as the gain from the VCO output to the CP output [9], the PLL open loop bandwidth $f_{\rm BW}$ can be expressed as

$$f_{\rm BW}\approx\frac{\beta_{\rm CP}\cdot R_1\cdot K_{\rm VCO}}{2\pi}. \quad (5)$$

Substituting (5) into (4) yields

$$\mathrm{SP}_{\rm fref,CP}\approx 20\log\frac{\left(\dfrac{f_{\rm pole}}{f_{\rm BW}}\right)}{2}+20\log\frac{i_{\rm CP,fref}}{\beta_{\rm CP}}+40\log\frac{f_{\rm BW}}{f_{\rm ref}}. \quad (6)$$

Therefore to reduce the CP-induced VCO spur, we can: 1) adopt a small $f_{\rm pole}/f_{\rm BW}$, but it is often limited by the phase margin requirement; 2) use a large $\beta_{\rm CP}$ or in other words use a small $R_1\cdot K_{\rm VCO}$ for a given $f_{\rm BW}$, but it increases filter capacitor area or reduces VCO analog tuning range; 3) reduce the CP output current ripple $i_{\rm CP,fref}$; 4) use a small loop-bandwidth-to-reference-frequency ratio $f_{\rm BW}/f_{\rm ref}$ to have more ripple suppression. For a given $f_{\rm ref}$, there is thus a tradeoff between low VCO spur and large $f_{\rm BW}$. For a given spur requirement, a CP design with lower ripple enables the use of a higher $f_{\rm BW}$, which is often desired as it offers faster settling time, and reduces on-chip loop filter area and sensitivity of the VCO to pulling. Fig. 2(b) shows a classical implementation of a low-ripple CP [8]. The current sources are implemented with cascoded transistors to boost the output impedance and improve matching. Another factor which also contributes to CP current ripple is the charge sharing between the parasitic capacitances at the current sources' drain nodes d1 and d2 and the LF capacitors if their voltages are not equal when they are connected during CP switching. The conventional CP in Fig. 2(b) uses a current-steering topology, where $I_{\rm UP}$ and $I_{\rm DN}$ are either connected to LF or dumped to $V_{\rm dump}$. An operational amplifier acting as unity gain buffer sets $V_{\rm dump}=V_{\rm LF}$. In this way, $I_{\rm UP}$ and $I_{\rm DN}$ are kept on all the time and the voltages on d1 and d2 are kept constant during CP switching, thereby minimizing the LF-CP charge sharing

B. Low Spur CP Using Sub-Sampling

Fig. 3(a) shows the top-level schematic of the SSPD/CP [9]. During operation, the SSPD directly samples the high-frequency VCO with the low-frequency Ref without using a frequency divider. It detects the phase difference between the

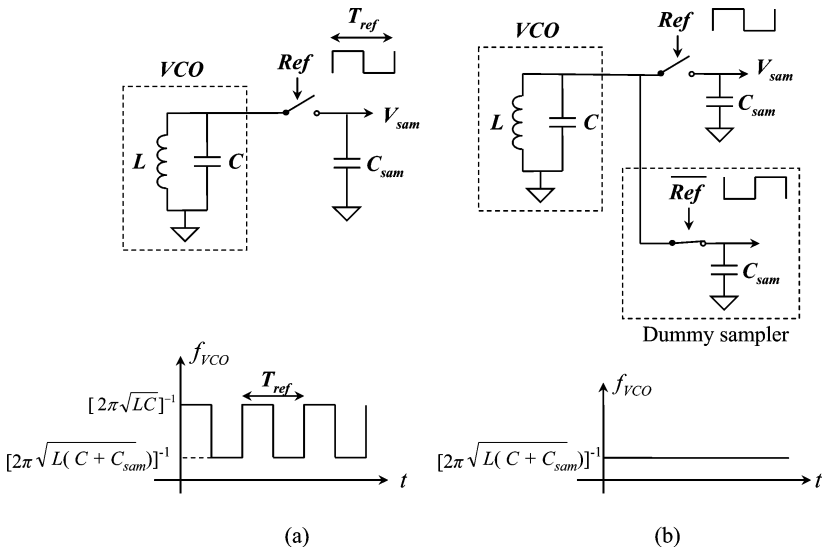

Fig. 4. (a) Simple model for VCO sampling. (b) VCO sampling with dummy sampler.

VCO and the Ref sampling edge and converts it into a sampled voltage difference $(V_{\mathrm{sam}+} - V_{\mathrm{sam}-})$, which is then used to control the amplitude of I_{UP} and I_{DN}. A block Pulser generates a pulse *Pul*, non-overlapping with Ref, and switches on/off I_{UP} and I_{DN} *simultaneously*. This Pulser controls the CP gain and also functions as the slave track-and-hold for the VCO sampling. Therefore, in this CP, I_{UP} and I_{DN} have *variable amplitudes* but a *constant on-time* equal to the on-time of the Pulser output τ_{pul}. Assuming ideal switching, the following equation must be satisfied to meet the steady-state locking condition of zero net CP output charge:

$$I_{\mathrm{UP}} \cdot \tau_{\mathrm{pul}} = I_{\mathrm{DN}} \cdot \tau_{\mathrm{pul}} \Rightarrow I_{\mathrm{UP}} = I_{\mathrm{DN}}. \tag{7}$$

In other words, I_{UP} and I_{DN} must have equal amplitude and the I_{UP} and I_{DN} mismatch is eliminated in this CP.[1] Actually, there is always mismatch between I_{UP} and I_{DN} if they are implemented with MOS transistors. However, the SSPLL loop tunes $V_{\mathrm{sam}+}$ and $V_{\mathrm{sam}-}$ until the amplitudes of I_{UP} and I_{DN} match, by shifting the sampling/locking point away from the ideal point (VCO zero-crossing); see Fig. 3(a). So the mismatch between the current sources' transistors still causes static phase error as in a conventional CP, but here it does not generate CP output current ripple.

Fig. 3(b) shows the proposed low-ripple CP design which is much simpler than the conventional one in Fig. 2(b). Since I_{UP} and I_{DN} mismatch will be tuned out by the PLL loop, the current sources' output impedance is not an issue and single transistors are used, which saves voltage headroom. While the conventional CP needs a unity-gain buffer to keep $V_{\mathrm{dump}} = V_{\mathrm{LF}}$ and minimize CP-LF charge sharing, we discovered that here this can be achieved by just connecting an extra capacitor C_{dump} to the current dumping node as explained below. In steady state, the net charge into the LF and C_{dump} should be both zero. Since I_{UP} and I_{DN} have equal on-time in both 'connected to LF' and 'connected to C_{dump}' cases, they must also have equal amplitude in both cases. This condition is met only when $V_{\mathrm{dump}} = V_{\mathrm{LF}}$ where the finite current source output impedance is actually the equalizing mechanism. When the drain nodes of the pMOS current source I_{UP} and nMOS current source I_{DN} are connected together, there is only one drain node voltage satisfying $I_{\mathrm{UP}} = I_{\mathrm{DN}}$ due to the finite current-source output impedance.

[1]This assumes ideal current source switches. In practice, there is also mismatch between the switches. Due to the finite rise and fall time of *Pul*, this causes mismatch in I_{UP} and I_{DN} switch-on time and thus mismatch in I_{UP} and I_{DN} amplitudes. If this is the limiting factor for VCO spur, the Pulser and the two switches which acts as the slave track and hold for VCO sampling can be removed and instead a second switch-capacitor circuit can be added to the SSPD. The CP is then always connected to the LF and no switching is needed. However, we will see that the CP is not anymore the major spur source in this SSPLL. It is therefore still beneficial to keep the Pulser as it simplifies the SSPD design and can be used to control the CP gain [9].

III. Spur Due to VCO Sampling and Techniques to Reduce It

In the previous section, we have shown that the amplitude-controlled CP in the SSPLL is inherently insensitive to mismatch and produces small ripple. In the design of [9], a CP based on the same principle was used. However, a rather poor −46 dBc reference spur was measured. Research shows that this is because the SSPD disturbs the VCO operation, via periodically changing the VCO capacitive load, charge injection from the sampling switch to the VCO and charge sharing between the VCO tank and the sampling capacitor. In the sub-sections below, we will analyze these VCO sampling spur mechanisms and propose techniques to suppress them. We will use a simplified diagram as shown in Fig. 4(a), where an ideal *LC* tank is directly sampled by Ref via a switch-and-capacitor SSPD. In the real design, a buffer will be added between the VCO and SSPD for isolation. To simplify the analysis and gain insights, we will firstly ignore the buffer and discuss the effect of the buffer later.

A. BFSK Effect

For an ideal sampler, the sampling clock should be a Dirac pulse with an infinitesimal duration time. As this requires an unpractical virtually zero duty cycle clock, a practical sampler is

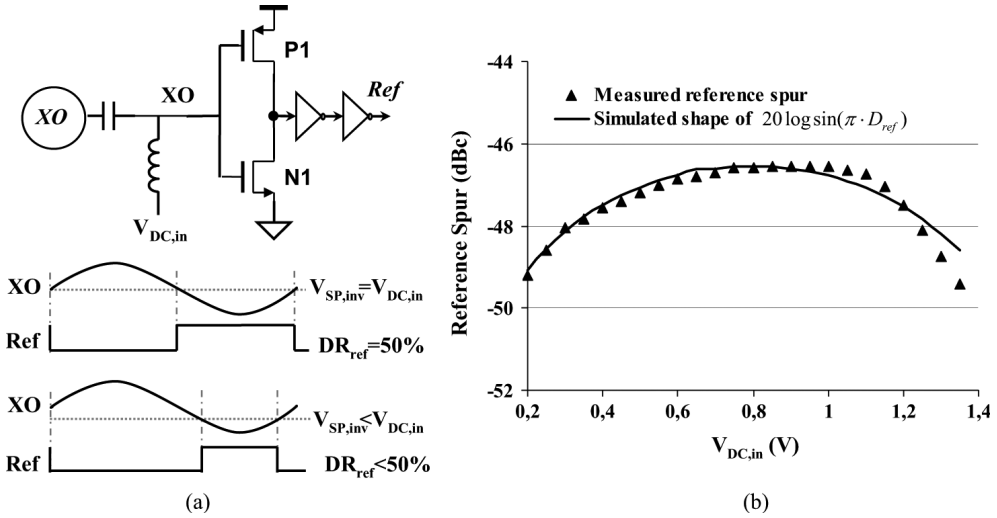

Fig. 5. (a) Schematic and timing diagram of inverter buffer, where $V_{\mathrm{SP,inv}}$ is the inverter switching point voltage. (b) Measured spur variations while tuning the position of Ref tracking edge via tuning $V_{\mathrm{DC,in}}$ from the design in [9].

usually implemented using a track-and-hold driven by a block-waveform with more practical duty-cycle as in Fig. 4(a). When Ref turns on the switch, the sampling capacitor C_{sam} is connected to the VCO and becomes part of the VCO loading. When Ref turns off the switch, C_{sam} is disconnected and the VCO is not loaded by C_{sam}. Therefore, the periodic switching of the sampler at frequency f_{ref} modulates f_{VCO} in a way similar to the case of binary frequency shift keying (BFSK) as shown in Fig. 4(a). Assuming $C_{\mathrm{sam}} \ll C_{\mathrm{tank}}$, the resulting VCO reference spur can be calculated as (see the Appendix)

$$\mathrm{SP}_{\mathrm{fref,BFSK}} = 20\log\left[\sin(\pi\cdot D_{\mathrm{ref}})\cdot\frac{N}{2\pi}\cdot\frac{C_{\mathrm{sam}}}{C_{\mathrm{tank}}}\right] \quad (8)$$

where D_{ref} is the Ref duty cycle. When there is a buffer between the VCO and SSPD as in [9], C_{sam} in (8) should be replaced by the effective capacitance change seen by the VCO due to Ref switching.

Equation (8) indicates that the BFSK effect induced reference spur varies with $\sin(\pi\cdot D_{\mathrm{ref}})$, which is used here to verify whether it is the dominant spur source. In [9], inverters as shown in Fig. 5(a) are used to convert the sine wave crystal oscillator (XO) into a steep square wave Ref. Now, the XO output is DC biased to $V_{\mathrm{DC,in}}$ with an off-chip bias-T and D_{ref} can be tuned by tuning $V_{\mathrm{DC,in}}$. Fig. 5(b) shows the measured reference spur variations of the design of [9] while tuning $V_{\mathrm{DC,in}}$. The shape matches well with the simulated $20\log\sin(\pi\cdot D_{\mathrm{ref}})$. We can conclude here that the BFSK effect is the major cause of the poor reference spur in [9].

In order to suppress the BFSK effect, we propose to add a dummy sampler as displayed in Fig. 4(b). The dummy sampler is a copy of the existing sampler but is controlled by the inverted Ref. Due to the complementary switching of the sampler and its dummy, the VCO is always connected to one C_{sam}. The VCO capacitive load thus does not change over time and the BFSK effect is compensated. In reality, this compensation is not perfect due to mismatch in the sampling capacitor ΔC_{sam}. Since the value of ΔC_{sam} is proportional to the square root of C_{sam}, (8) becomes

$$\mathrm{SP}_{\mathrm{fref,BFSK}} = 20\log\left[\sin(\pi\cdot D_{\mathrm{ref}})\cdot\frac{N}{2\pi}\cdot\frac{A_C\sqrt{2C_{\mathrm{sam}}}}{C_{\mathrm{tank}}}\right] \quad (9)$$

where A_C is a process constant describing the matching property of the sampling capacitor. The $\sqrt{2}$ factor rises because it is the mismatch between two C_{sam}. It is thus desirable to have a small C_{sam} for a low spur level. However, a smaller C_{sam} means a larger kT/C_{sam} and more sampler noise [9]. There is thus a tradeoff between the spur level and the in-band phase noise due to the SSPD.

B. Charge Sharing/Injection

Apart from the BFSK effect, the VCO sampling activity also brings two other mechanisms which disturb the VCO operation, namely charge injection from the sampling switches to the VCO and charge sharing between the VCO and C_{sam}. While the former can be canceled by adding dummy switches[6], [7], the latter needs more effort to deal with. The VCO-C_{sam} charge sharing occurs because the voltages on C_{sam} and the VCO tank capacitor may not be equal when they are connected at the switch-on moment, which can be explained using Fig. 6. Without loss of generality, we assume that the sampling switch is on when Ref is low and off when Ref is high (PMOS switches are used in the design for practical reasons). The Ref rising edge is then the sampling edge, i.e., the moment of switch-off where holding starts and voltage is sampled. The Ref falling edge is the tracking edge, i.e., the moment of switch-on where tracking starts. After the PLL achieves locking, the Ref sampling edge is aligned with a VCO zero-crossing. The voltage on C_{sam} at the switch-on moment is then well-defined and equal to the VCO DC voltage: $V_{\mathrm{sam,on!}} = V_{\mathrm{VCO,DC}}$, where the symbol "!" is used to stress the specific moment in time. In contrast, the voltage on the VCO tank capacitor at the switch-on moment $V_{\mathrm{VCO,on!}}$ depends on the position

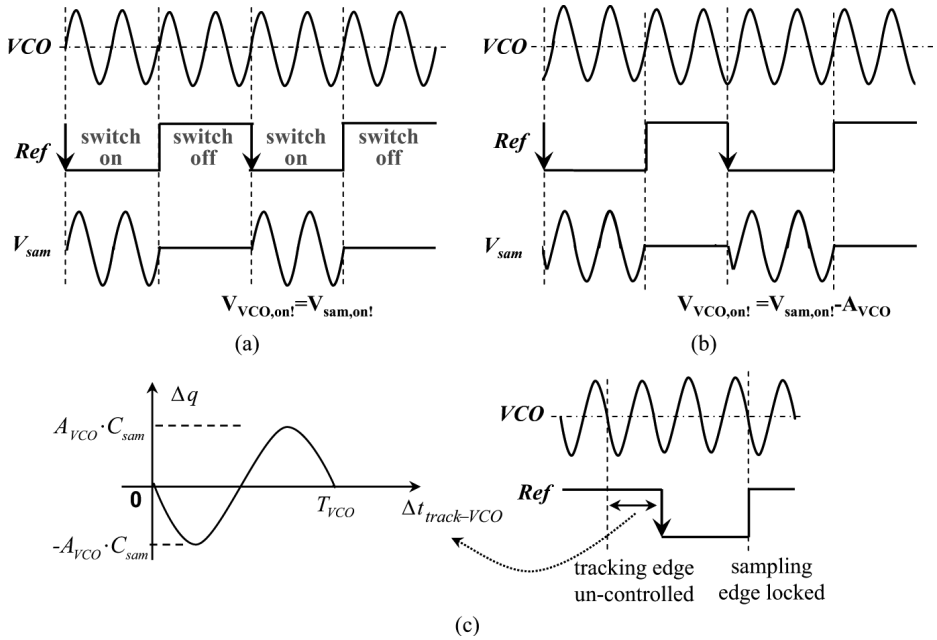

Fig. 6. Conceptual illustration of (a) the case of minimum charge sharing; (b) the case of maximum charge sharing; (c) amount of charge sharing when the relative position of the Ref falling edge and VCO zero-crossing changes.

of the Ref tracking edge which is ill-defined.[2] When the Ref tracking edge occurs at the VCO zero-crossings as shown in Fig. 6(a), we have $V_{\mathrm{VCO,on!}} = V_{\mathrm{sam,on!}} = V_{\mathrm{VCO,DC}}$ and hence no VCO-C_{sam} charge sharing. When the Ref tracking edge occurs at the VCO peaks as shown in Fig. 6(b), we have $V_{\mathrm{VCO,on!}} = V_{\mathrm{sam,on!}} - A_{\mathrm{VCO}}$ and maximum charge sharing. Using the simplified model in Fig. 4(a) and assuming $C_{\mathrm{sam}} \ll C$, the amount of charge sharing can be calculated as

$$\begin{aligned}\Delta q &\approx (V_{\mathrm{VCO,on!}} - V_{\mathrm{VCO,DC}}) \cdot C_{\mathrm{sam}} \\ &= A_{\mathrm{VCO}} \cos(2\pi f_{\mathrm{VCO}} \cdot \Delta t_{\mathrm{track-VCO}}) \cdot C_{\mathrm{sam}}. \quad (10)\end{aligned}$$

When the relative position of the Ref tracking edge and VCO zero-crossing $\Delta t_{\mathrm{track-VCO}}$ changes, Δq follows the VCO waveform and is periodic as shown in Fig. 6(c). Since more charge sharing means more disturbance to the VCO, qualitatively we can expect the VCO spur due to charge sharing to vary in a periodic pattern when we change $\Delta t_{\mathrm{track-VCO}}$. This will be discussed further in the measurement part in Section V.

It is worth noting that, in contrast to the case with the CP, all the aforementioned SSPD spur mechanisms disturb the VCO without going through the PLL loop filter. In other words, the loop filter renders no filtering for the SSPD caused spur and there is no tradeoff between low (SSPD caused) spur and high PLL bandwidth.

C. Low Spur PLL Architecture

From the previous section, it is clear that if we can tune the Ref tracking edge such that it is also aligned to a VCO zero-crossing, there is ideally no VCO-C_{sam} charge sharing. For the SSPLL, the timing of the Ref sampling edge is highly critical

[2]It is determined by the distance between the two Ref edges, i.e., determined by the Ref duty cycle which is uncontrolled at this stage.

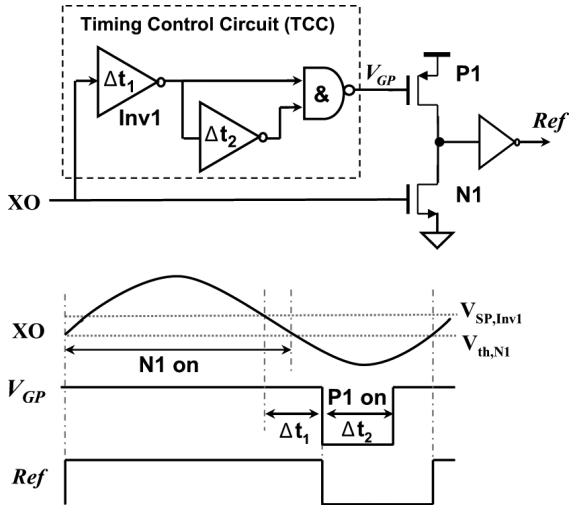

Fig. 7. Schematic and timing diagram of the proposed duty-cycle-controlled Ref buffer.

while the tracking edge is hardly relevant. It is thus desired to leave the sampling edge alone while tuning the tracking edge. With the simple inverter Ref buffer in Fig. 5(a), the Ref falling edge can be tuned by tuning $V_{\mathrm{DC,in}}$ but it also changes the timing of the Ref rising edge. Fig. 7 shows a modified inverter buffer which can solve this problem. The inverter nMOS N1 is directly connected to XO as in a conventional inverter, while a timing control circuit (TCC) is inserted between the pMOS P1 and the XO. The TCC generates a narrow pulse V_{GP} from the XO and controls the gate of P1. Δt_1 and Δt_2 are set such that the time when V_{GP} is low (P1 conducts) and the time when XO is higher than the threshold of N1 (N1 conducts) is non-overlapping. In this way, the Ref rising edge is defined by XO via N1 while the Ref falling edge is independently defined by V_{GP} via

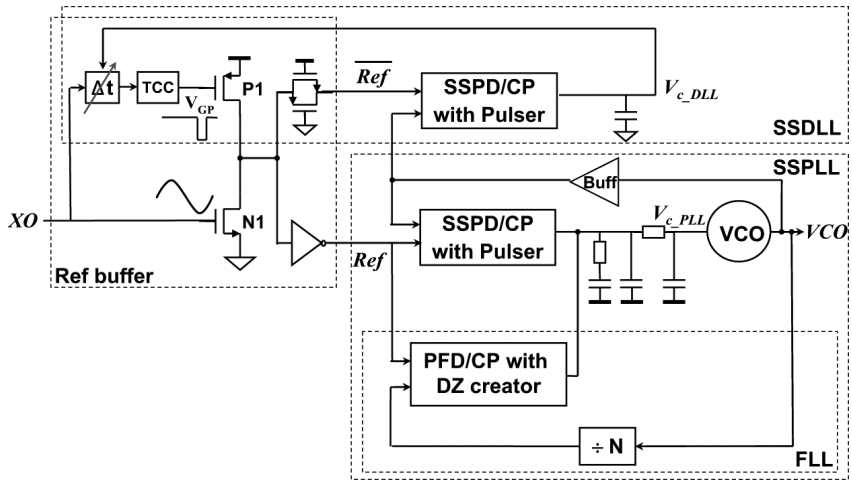

Fig. 8. Block diagram of the low-spur PLL.

P1 (and the inverter thereafter). The Ref falling edge can then be tuned by tuning Δt_1, without affecting the Ref rising edge.

In order to align the Ref falling edge with the VCO zero-crossing, we also need a phase detector to detect the phase difference between them. The dummy sampler in Fig. 4(b) serves this purpose well since it operates in a complementary way and uses the $\overline{\text{Ref}}$ rising edge, i.e., Ref falling edge as its sampling edge. Fig. 8 shows the proposed low-spur PLL architecture. The core is a SSPLL similar to the one in [9]. It uses a SSPD that utilizes the Ref rising edge to sample the VCO and thus aligns the Ref rising with a VCO zero-crossing. On top of the SSPLL, a sub-sampling delay-locked loop (SSDLL) is added which uses the same SSPD/CP as the SSPLL, but its sampling clock $\overline{\text{Ref}}$ is the inverse of Ref. A transmission gate compensates the inverter delay. The SSDLL thus uses the $\overline{\text{Ref}}$ rising edge to sample the VCO and aligns the $\overline{\text{Ref}}$ rising edge, i.e., the Ref falling edge to the VCO zero-crossing. Now, both the Ref rising and falling edges are aligned with the VCO zero-crossings and the condition for no VCO-C_{sam} charge sharing is achieved. Moreover, the SSPD/CP in the SSDLL acts as a dummy for the SSPD/CP in the SSPLL which compensates the BFSK effect and cancels the charge injection from the sampling switches to the VCO. Therefore, all the three aforementioned SSPD-related spur mechanisms are largely suppressed. Since the SSDLL tuning only affects the timing of the Ref falling edge, which is the noncritical edge for the SSPLL, it will neither disturb the SSPLL operation nor add noise to the SSPLL output.

For simplicity, the above spur analysis assumed that the SSPD is directly connected to the VCO. In practice, buffers can be added between the SSPD and VCO to provide isolation. However, practical buffers have limited isolation due to e.g., parasitic capacitors. The SSPD will still disturb the VCO via parasitic paths and the insights developed for SSPD spur mechanisms in the case of no buffer remain useful design guidelines. The proposed techniques (dummy sampler, DLL tuning) provide extra spur reduction in addition to the use of buffering, and thus relax the buffering needs while achieving a certain spur level. This saves power as buffers running at f_{VCO} are power consuming. In the design described here we do use a buffer (described in Section IV) in order to demonstrate very low spur. In [17] we show a different design exploiting this power advantage to its maximum by removing buffering for isolation completely.

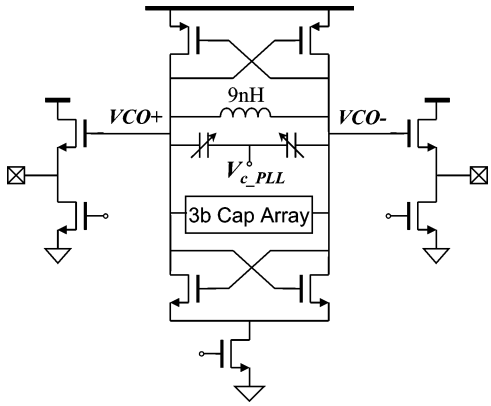

Fig. 9. Schematic of the VCO.

IV. Design and Implementation

A. VCO

Fig. 9 shows the schematic of the VCO. In order to make a direct comparison with [9] and demonstrate the effectiveness of the spur reduction techniques, the same VCO as in [9] is used, which is a tail-biased one with a double switch pair and an inductor of 9 nH.[3] The VCO has a 50 MHz/V analog tuning gain and a 3-bit digital controlled capacitor bank to increase the frequency range to overcome process spread. It consumes 1 mA from a 1.8 V supply.

B. SSPD/CP With Pulser

Fig. 10 shows the schematic of the SSPD/CP with Pulser. Aiming at very low spur, a two-stage CML inverter is used as a buffer to isolate the VCO from the SSPD. The sampling capacitor in the SSPD has a value of 10 fF. A 2 kΩ passive resistance R_{sam} is added in series with the MOS switch on the

[3]The inductor used here has a large value. To lower the spur level, a smaller coil could be used so that the tank capacitor can be larger which reduces the sensitivity of the VCO to the SSPD spur mechanisms.

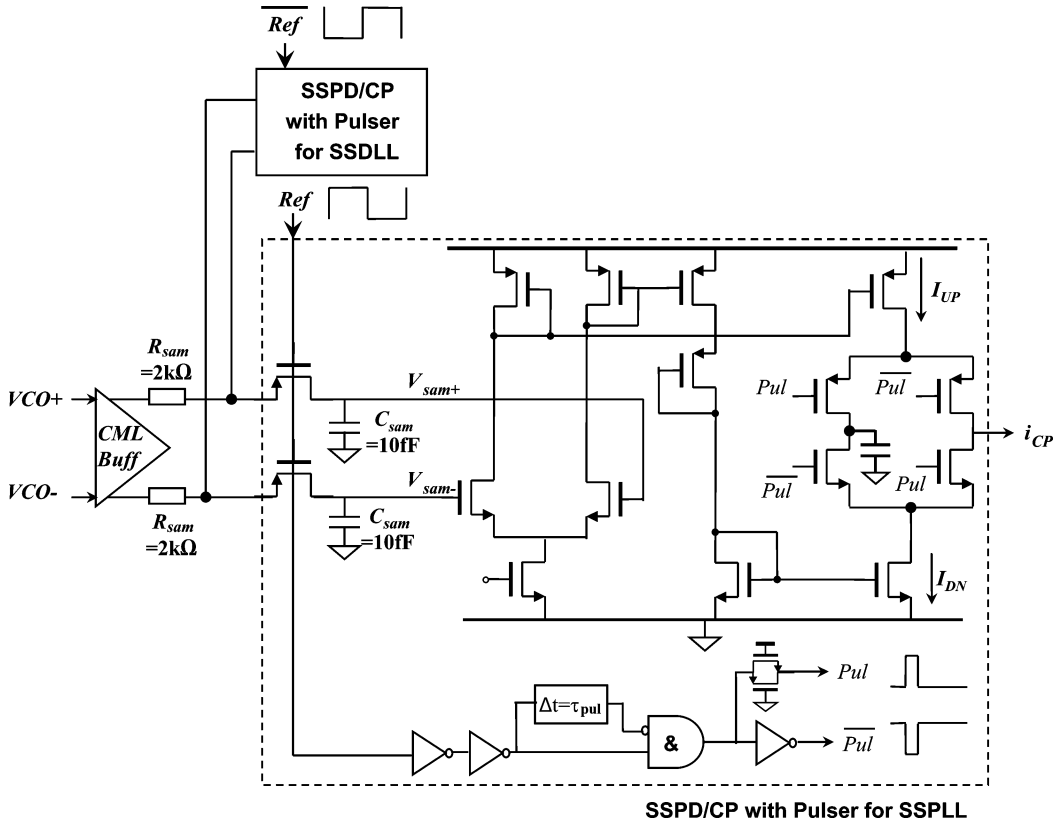

Fig. 10. Schematic of the SSPD/CP with Pulser.

shared path of the SSDLL and SSPLL, which serves two purposes. Because $C_{\rm sam}$ is charged and discharged by the MOS switch, the on-resistance of the MOS switch plays a role in the transient behavior. By setting the value of $R_{\rm sam}$ to be larger than the on-resistance of the MOS switch, the overall on-resistance will be governed by $R_{\rm sam}$. Since $R_{\rm sam}$ is shared, the mismatch between the on-resistance of the two SSPDs is reduced, leading to a better matching in the SSPD *RC* constant. Secondly, the sine-wave VCO becomes more like square wave after the CML buffer, which reduces the linear range of the SSPD. The added $R_{\rm sam}$ together with $C_{\rm sam}$ also forms a low-pass filter and brings the waveform back to sine-wave-like before it is sampled by the SSPD. Since the noise contribution of the SSPD is governed by kT/C, adding $R_{\rm sam}$ will not increase the SSPD noise.

The CP consists of two stages. The first stage is a differential pair converting the sampled voltage into current and the second stage has been explained in Fig. 3(b). The CP up- and down-current sources are biased at 20 μA. The current source switches use near minimum size and the dumping capacitor is set to 2.5 pF, to reduce the effect of clock feed-through and charge injection.

C. SSDLL

The schematic of the SSDLL is displayed in Fig. 11. The tunable delay cell is implemented with a current starved inverter and its tuning range is designed to cover one VCO period with margin, which is enough for the SSDLL to align the Ref falling edge with a VCO zero-crossing. The rest of the Ref buffer has been shown in Fig. 7.

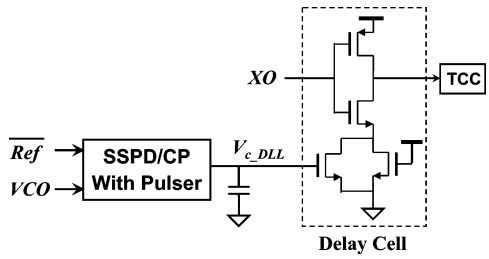

Fig. 11. Schematic of the SSDLL.

D. Settling Behavior

The overall architecture in Fig. 8 includes multiple loops: a SSPLL core loop, a FLL for frequency locking which consists of a divider, and a three-state PFD/CP with a built-in $(-\pi, \pi)$ dead zone (DZ) [9], and a SSDLL for Ref duty cycle tuning. Since the SSDLL only tunes the Ref tracking edge, it will not affect the loop dynamics of the SSPLL. The delay of the DLL delay cell is set to the middle of its tuning range at start-up.

Fig. 12 shows the transient simulation results for the overall system. During frequency acquisition, $f_{\rm VCO}$ is much different from $N \cdot f_{\rm ref}$. The FLL dominates the loop dynamic and charges up the loop filter. There are several noticeable regions where the FLL is doing nothing. That is because even though the frequency error is not yet zero, the instantaneous phase error can be smaller than π and falls inside the DZ. The CP in the FLL thus injects no current into the loop filter. Since there is still a frequency error, the phase error keeps accumulating until it becomes larger than π and falls outside the DZ. The FLL then takes action again. After the core SSPLL loop achieves locking, the frequency error

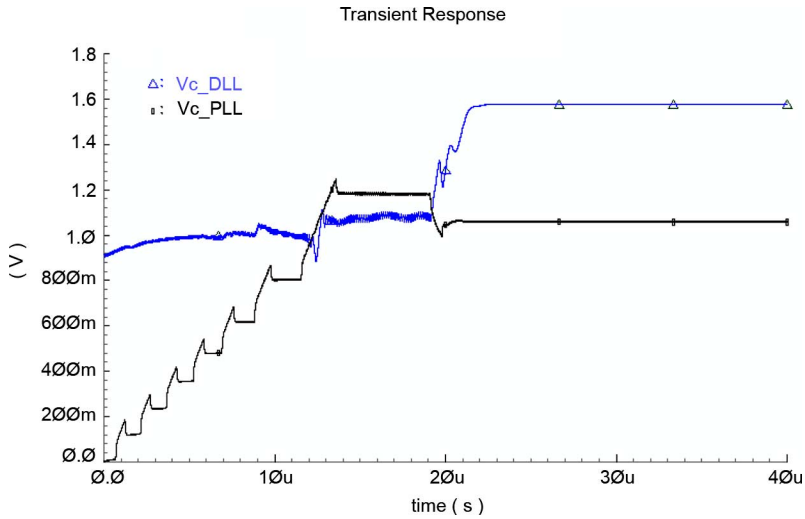

Fig. 12. Settling behavior of the overall system.

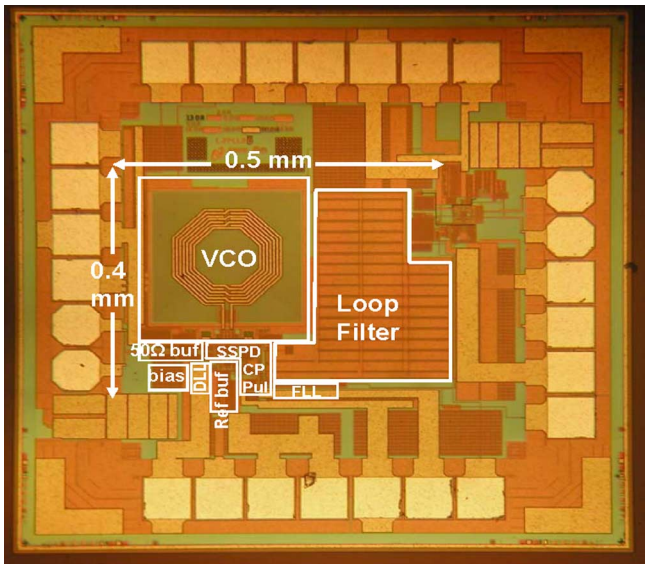

Fig. 13. Chip microphotograph.

is zero and the phase error is always small. The FLL stays quiet and injects nothing to the filter. The SSDLL settles later than the SSPLL since we set its bandwidth to be smaller than that of the SSPLL. For experimental purposes, the SSDLL tuning can be disabled from off-chip by connecting its filter capacitor to half supply instead of its CP.

V. Experimental Results

To verify the presented ideas, a 2.21 GHz SSPLL, according to Fig. 8, has been fabricated in a standard 0.18 μm CMOS process and tested in a 24 pin Quad LLP package. Fig. 13 shows a die microphotograph, with an active area of 0.4 $\times$ 0.5 mm^2. All circuitry uses a 1.8 V battery supply, while separate supply domains provide isolation. The reference clock is derived from a low-noise 55.25 MHz crystal oscillator from Wenzel Associates. The crystal oscillator output is attenuated to 1.8 V_{pp} and DC biased using a bias-T before it is fed into the chip.

The PLL core (excluding the 50 Ω buffer) consumes 3.8 mW, with less than 0.2 mW in the SSDLL. Fig. 14 shows the measured phase noise spectrum using an Agilent E5501B phase noise measurement setup. The in-band phase noise is -121 dBc/Hz at 200 kHz offset and out-of-band phase noise is -138 dBc/Hz at 20 MHz offset. Enabling the SSDLL does not increase the phase noise level. Compared with [9], the in-band phase noise is 5 dB higher, mainly because we used one more SSPD buffer stage and a 6x smaller $C_{\rm sam}$ in this design which helps reducing the spur level but raises the noise contribution of the SSPD and its buffer. According to the noise summary in Spectre RF Noise simulations, the reference clock (XO and buffer), the SSPD and its buffer, and the rest of the circuits contribute 30%, 55%, and 15% to the in-band phase noise at 200 kHz, respectively. Due to this higher in-band phase noise and a less optimally designed loop bandwidth, it also has a higher jitter than [9]: 0.3 $\rm ps_{rms}$ integrating from 10 kHz to 100 MHz. However, the jitter/power figure-of-merit (FOM) [18] of this design is still competitive compared to the best low-jitter PLL designs we found in ISSCC and JSSC papers as shown in Fig. 15, even though our design is not optimized for jitter but for a low reference spur.[4]

In [10], we showed measurement results for reference spurs from 20 chips. Here we measured 20 additional chips for spurs at $f_{\rm ref}$ (reference spur) as well as spurs at $2f_{\rm ref}$ away from the VCO frequency with the SSDLL enabled. The results are shown in Fig. 16(a). The spurs at $2f_{\rm ref}$ are actually a few dB higher than the spurs at $f_{\rm ref}$. That is because with the complementary switched dummy sampler added, the SSPD switching on/off activity is doubled. This does not affect the BFSK effect since $f_{\rm VCO}$ still changes once every Ref period. However, the charge injection/sharing now happens twice every Ref period. Therefore, we can expect to see spurs at $f_{\rm ref}$ as well as $2f_{\rm ref}$. From Fig. 16(a), we see that the worst sample has <-76 dBc at $2f_{\rm ref}$ and <-80 dBc at $f_{\rm ref}$. The reference spur is thus >34 dB better

[4]The reference spurs for the low-jitter PLL designs in [9] and [19]–[23] are either not reported or larger than -65 dBc. Therefore, they are not included in the reference spur comparison in Table I.

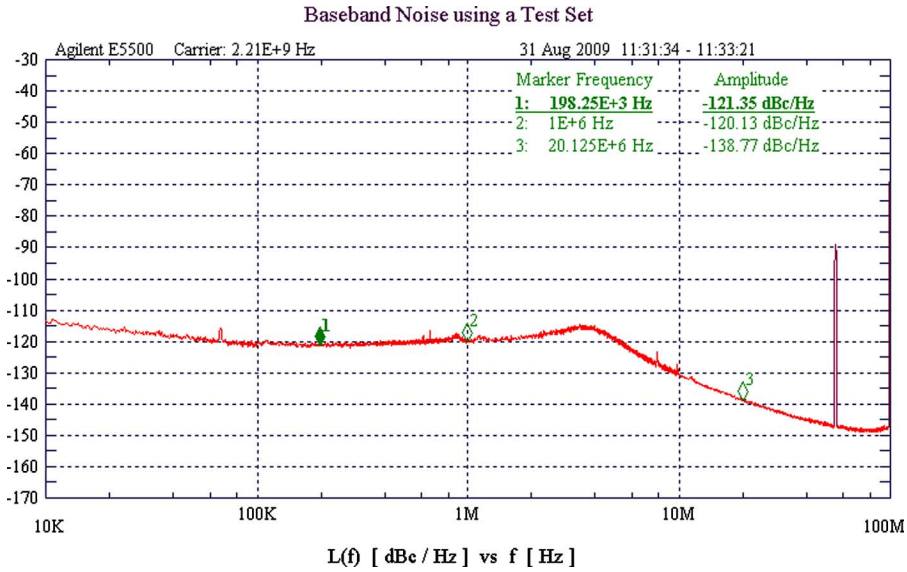

Fig. 14. Measured PLL phase noise.

TABLE I
SSPLL PERFORMANCE SUMMARY AND COMPARISON WITH LOW SPUR PLL DESIGNS.

	This work	[2]	[3]	[5]	[6]*	[7]*	[24]	[25]
f_{out} (GHz)	2.21	5.5	5.4	5.2	2.4	3.6	5.24	5.3
f_{ref} (MHz)	55.25	43	10	10	12	50	13.33	20
f_{BW}/f_{ref}	1/20	1/540	1/400	1/50	1/12	1/50	1/66	1/333
Spur@f_{ref}/2f_{ref} (Sample #)	<-80/<-76 (#=20)	-69 (#=1)	-70 (#=1)	-69 (#=1)	-70 (#=4)	-74 (#=1)	-66 (#=1)	-74 (#=1)
In-band phase noise (dBc/Hz)	-121@ 200kHz	-88@ 40kHz	-63@ 10kHz	-76@ 20kHz	-103@ 100kHz	-98@ 100kHz	-95@ 40kHz	-79@ 10kHz
Power (mW)	3.8	23	13.5	19.8	39	110	56	36
Active area (mm^2)	0.20	?	0.49	0.64	<4.8	2.7	?	0.8
Technology	0.18-µm CMOS	0.25-µm CMOS	0.25-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS

*These two are Fractional-N PLLs. The numbers for [6] are measured in Integer-N mode.

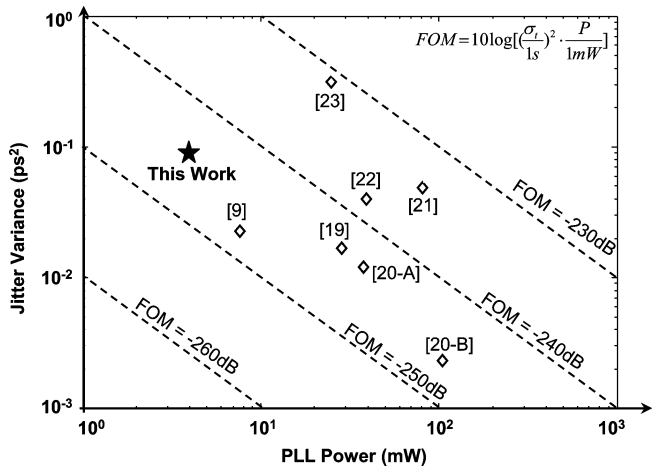

Fig. 15. Jitter and power comparison between this work and other good FOM PLLs.

than [9]. The spectrum of the chip with the lowest spurs is shown in Fig. 17.

To investigate the effect of the SSDLL on the spur level, the VCO spurs have been measured with the SSDLL enabled and disabled while tuning the position of the Ref falling edge via changing $V_{\mathrm{DC,in}}$. The result is shown in Fig. 16(b). When the SSDLL is disabled, the spurs show a periodic pattern when the relative position of the Ref tracking edge and VCO zero-crossing is changed by T_{VCO}[5]. Note that when the SSDLL is disabled by disconnecting its loop filter and the tunable delay cell, its SSPD still functions as the dummy for the SSPD of the SSPLL and helps to reduce the spur level. When the SSDLL is enabled, the spurs hardly change with $V_{\mathrm{DC,in}}$ which indicates that the DLL tuning works. The DLL tuning has a larger effect on spur at f_{ref} than at $2f_{\mathrm{ref}}$ because it only tunes the Ref tracking edge which occurs once every Ref period. The spur level with the SSDLL enabled (corresponding to minimum charge sharing in theory) is not the lowest but close to the average. This can be explained if the charge sharing has comparable contribution as the other spur mechanisms. Depending on the relative position of the Ref falling edge and the VCO zero crossing, the sign of charge sharing can be positive or negative (C_{sam} injects charge to or absorbs charge from the VCO; see Fig. 6). It thus may add up or cancel the other spur sources, thereby increasing or reducing the spur level. Although enabling the SSDLL does not

[5]In measurement, it is not possible to see how much the Ref tracking edge is shifted on-chip with a certain change in $V_{\mathrm{DC,in}}$. Simulation is thus used to estimate the shifts of Ref falling when $V_{\mathrm{DC,in}}$ is tuned from 0.5 V to 0.6 V in Fig. 16(a). It can only be a coarse estimation as the measured sample is subject to PVT variations.

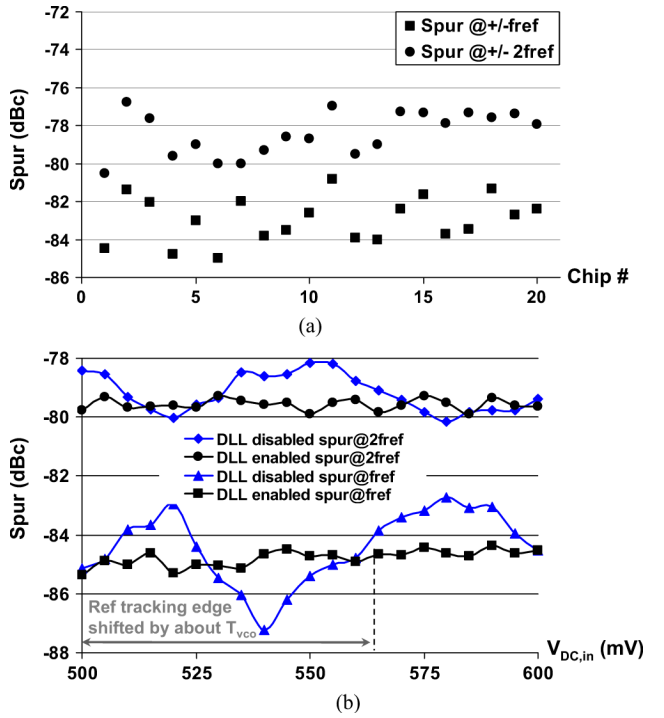

Fig. 16. (a) Spurs measured from 20 chips with SSDLL tuning enabled. (b) Measured spur variations while tuning the position of Ref tracking edge via tuning $V_{\mathrm{DC,in}}$.

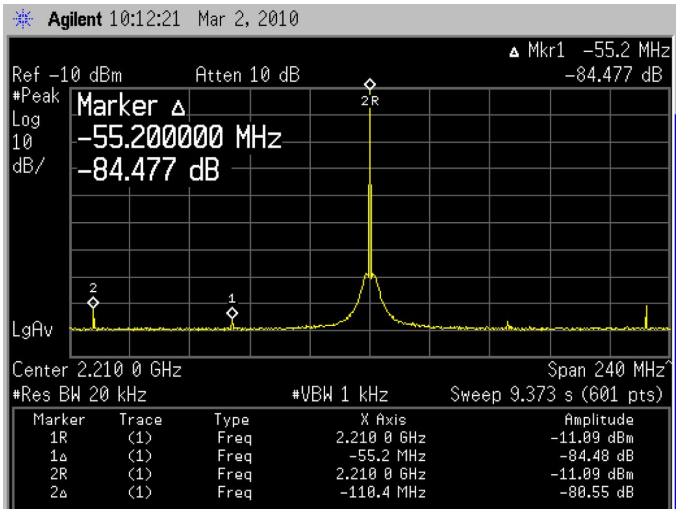

Fig. 17. Spectrum of the chip with the lowest spurs in Fig. 16(a).

result in the lowest spur, it is still valuable as it improves the worst case spur. The improvement is limited in this case, but reduced variability is still valuable. The power and area overhead of having the DLL tuning is also small.

Table I summarizes the PLL performance and displays a comparison with other low-spur PLLs. This design has the lowest spur combined with lower in-band phase noise and power consumption. Note that we measured 20 samples and the low spur is achieved with a high $f_{\mathrm{BW}}/f_{\mathrm{ref}}$ of 1/20. The measurement results in Fig. 16 suggest that the spur level is still limited by the SSPD, not the CP. The PLL bandwidth can thus be increased even further without increasing the spur level. When an even lower spur level is desired, more buffering or buffers with better isolation (than the two-stage CML buffer here) may be used to further isolate the VCO from the SSPD.

VI. Conclusion

Design techniques to reduce the PLL reference spur have been proposed. By exploiting sub-sampling phase detection, the CP can be amplitude controlled and insensitive to mismatch. Low CP ripple can thus be achieved with a simple design. With the CP ripple reduced, the main source of VCO spur is the SSPD sampler which periodically disturbs the VCO operation via charge injection, charge sharing and frequency modulation due to a change in the VCO capacitive load. In contrast to the CP-induced spurs, the spur due to periodic sampling of the VCO is not related to the loop filter and there is thus no tradeoff between high loop bandwidth and low spur. Dummy samplers and isolation buffers are used to minimize the disturbance of the SSPD and the VCO. A duty-cycle-controlled reference buffer with DLL tuning is proposed to further reduce the worst case spur level. While using a high loop-bandwidth-to-reference-frequency ratio of 1/20, the reference spurs measured from 20 chips are <-80 dBc. Since the frequency divider noise is eliminated and the SSPD and CP noise is not multiplied by N^2, the sub-sampling-based PLL also has good phase noise performance. It achieves -121 dBc/Hz at 200 kHz in-band phase noise with only 3.8 mW power. The output jitter integrated from 10 kHz to 100 MHz is 0.3 $\mathrm{ps_{rms}}$.

Appendix
VCO Spur Due to BFSK Effect

This Appendix aims at estimating the VCO spur level due to the SSPD BFSK effect. Due to the SSPD switching, f_{VCO} is time varying as shown in Fig. 4(a). The VCO waveform in this case can be expressed as

$$v_{\mathrm{VCO}}(t) = A_{\mathrm{VCO}} \cos\left[2\pi f_{\mathrm{VCO,avg}} t + \int 2\pi \Delta f_{\mathrm{VCO}}(t) dt\right] \tag{11}$$

where A_{VCO} is the VCO amplitude and $f_{\mathrm{VCO,avg}}$ is the average VCO frequency which is locked to $N \cdot f_{\mathrm{ref}}$ by the PLL. $\Delta f_{\mathrm{VCO}}(t)$ is the difference between the instantaneous VCO frequency and $f_{\mathrm{VCO,avg}}$ and has the same shape as the Ref waveform. Using Fourier transform, the fundamental harmonic content of $\Delta f_{\mathrm{VCO}}(t)$ can be calculated as

$$\Delta f_{\mathrm{VCO}}(t) = \frac{2}{\pi} \cdot \Delta f_{\mathrm{VCO,pp}} \cdot \sin(\pi \cdot D_{\mathrm{ref}}) \cdot \cos(2\pi f_{\mathrm{ref}} t) \tag{12}$$

where D_{ref} is the Ref duty cycle and $\Delta f_{\mathrm{VCO,pp}}$ is the peak-to-peak amplitude of $\Delta f_{\mathrm{VCO}}(t)$. Assuming $C_{\mathrm{sam}} \ll C_{\mathrm{tank}}$, we have

$$\begin{aligned} \Delta f_{\mathrm{VCO,pp}} &\approx \frac{C_{\mathrm{sam}}}{2C_{\mathrm{tank}}} \cdot f_{\mathrm{VCO,avg}} \\ &= \frac{C_{\mathrm{sam}}}{2C_{\mathrm{tank}}} \cdot N \cdot f_{\mathrm{ref}}. \end{aligned} \tag{13}$$

Substituting (12) and (13) into (11), the VCO spur at f_{ref} offset, i.e., the VCO reference spur can be derived as

$$\mathrm{SP_{fref,BFSK}} = 20 \log\left[\sin(\pi \cdot D_{\mathrm{ref}}) \cdot \frac{N}{2\pi} \cdot \frac{C_{\mathrm{sam}}}{C_{\mathrm{tank}}}\right]. \tag{14}$$

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